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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/709,800	11/09/2000	Min-Cheng Kao	JCLA-6349	4354

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J.C. PATENTS INC.
4 VENTURE
SUITE 250
IRVINE, CA 92618

EXAMINER	
O'BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 10/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/709,800	KAO ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/09/00,4/02/01 and 9/14/01* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-16 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Information Disclosure Statement as received on 11/09/2000, Declaration and Surcharge Fee as received on 4/02/2001, and Change of Address as received on 9/14/2001.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The abstract of the disclosure is objected to because it contains legal phraseology such as "comprising". Correction is required. See MPEP § 608.01(b).

Drawings

5. The drawings are objected to because of the following:

a. In Figure 1, please change the label "multiplien" to correctly read "multiplier".

6. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

7. Claims 6, 8, 14 and 16 are objected to because of the following informalities:

a. Claim 6 recites the limitation "forth N-bit part". Please correct the limitation to read "fourth N-bit part". See also similar corrections in claims 8, 14 and 16.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-4, and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seal et al., U.S. Patent No. 5,583,804.

10. Regarding claims 1 and 9, taking claim 1 as exemplary, Seal has taught an apparatus for processing data (102 of Fig.1), said apparatus comprising:

a. A general register bank of N-bit data processing registers (106 of Fig.1);

b. A multiplier (108 of Fig.1 and 14,16,18,20 of Fig.6B) for performing multiply operations upon a first operand and a second operand and outputting a 2N-bit multiplied result (see Col.2 lines 58-65 and Col.17 lines 39-40);

c. An accumulator (108 of Fig.1), coupled to the multiplier and the general register bank (see Fig.1), for performing accumulate operations upon the 2N-bit

multiplied result and the 2N-bit addition operand and outputting a 2N-bit accumulated result (see Col.2 lines 3-8).

11. Seal has not explicitly taught a special bank of N-bit data processing registers, the selector coupled to the special register bank and the general register bank, for selecting one of the special and general register banks and outputting a selected N-bit result from the selected register bank, wherein the selected N-bit result and a N-bit data form a 2N-bit addition operand, as well as having not taught the accumulator coupled to the selector.

12. However, Seal has taught the general register bank (106 of Fig.1) having only two read ports and taking at least two cycles for a multiply-accumulate instruction to execute (see Col.5 lines 60-64). It is well known in the art that reducing the amount of cycles that instructions take to execute is of paramount concern. One of ordinary skill in the art at the time of the invention would have recognized that placing two register banks with two read ports each allows 4 read ports to be active at once. Therefore, it would have been obvious to one of ordinary skill in the art to combine two general register banks in parallel in order to read out twice as many operands in half as much time, reducing the amount of cycles a multiply-accumulate instruction takes to execute.

13. Furthermore, one of ordinary skill in the art would have recognized the requirement for a selector, such as a multiplexer, to be connected between the two general register banks and the accumulator, to mediate and recognize the data coming out of the banks so that data from the correct locations gets processed instead of being arbitrarily put on a data bus without identification. Thus, it would have been obvious to one of ordinary skill in the art at the time of

the invention to place a selector connected to the outputs of the two general register banks in order to choose the correct data from the correct locations after it has been read from the banks.

14. Claim 9 is nearly identical to claim 1, differing only in minor informalities in their claim language. Thus, claim 9 is rejected for the same reasons as claim 1.

15. Regarding claims 2 and 10, taking claim 2 as exemplary, Seal has taught the apparatus for processing data of claim 1, wherein the N-bit data is held in the general register bank (see Col.3 lines 59-60 and Col.4 lines 1-2). The third and fourth data processing registers are located within the general register bank (106 of Fig.1) (see Col.3 lines 48-55).

16. Claim 10 is nearly identical to claim 2, differing only in their parent claims, which are both rejected above. Thus, claim 10 is rejected for the same reasons as claim 2.

17. Regarding claims 3 and 11, taking claim 3 as exemplary, Seal has taught the apparatus for processing data of claim 1, wherein the selector selects one of the special and general register banks. Seal has not taught the selector receiving a class signal and then selecting one of the register banks in response to the signal.

18. However, Seal has taught a class signal which is used for indicating a first or second class of instruction (see 36 of Fig.2 and Fig.3, also Col.5 lines 13-15 and 44-47). Because the first and second classes of instructions require different numbers and combinations of operands to be read from the register banks (see Col.3 lines 56-67 and Col.4 lines 1-7), one of ordinary skill in the art would have recognized that class signal should be used in selecting the register bank from which the operands are coming. Therefore, it would have been obvious to one of ordinary skill in the art to control the selector between the register banks with a class signal so that the correct

register bank and operands could be selected based upon the class of an instruction being executed.

19. Claim 11 is nearly identical to claim 3, differing only in their parent claims, which are both rejected above. Thus, claim 11 is rejected for the same reasons as claim 3.

20. Regarding claims 4 and 12, taking claim 4 as exemplary, Seal has taught the apparatus for processing data of claim 3, the class signal is used for indicating a first class of instruction or a second class of instruction (see 36 of Fig.2 and Fig.3, also Col.5 lines 13-15 and 44-47), wherein the first class of instruction is executing a first calculation of N*N+2N→2N and the second class of instruction is executing a second calculation of N*N+N→N (see Col.2 lines 18-22).

21. Claim 12 is nearly identical to claim 4, differing only in their parent claims, which are both rejected above. Thus, claim 12 is rejected for the same reasons as claim 4.

22. Claims 5-8 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seal et al, U.S. Patent No. 5,583,804 as applied to claims 1, 4-5 and 8 above, and further in view of Morrison et al, U.S. Patent No. 6,581,086.

23. Regarding claim 5, Seal has taught the apparatus for processing data of claim 4, but has not taught the apparatus further comprising a detecting device, coupled to the accumulator, for receiving the 2N-bit accumulated result and for checking if a case of overflow occurs.

24. However, Morrison has taught a scaler (60 of Fig.9) connected to the accumulator (see Fig.9) that contains a comparator that determines whether the result has overflowed (see Col.9 lines 24-42). One of ordinary skill in the art would have recognized that overflow detection is desirable in order to prevent errors from propagating through a data processing system without

having to recalculate operations already performed (see Col.10 lines 54-58). Therefore, one of ordinary skill in the art at the time of invention would have found it obvious to include a comparator connected to the accumulator to detect overflow to prevent error propagation.

25. Claim 13 is nearly identical to claim 5, differing only in their parent claims, which are both rejected above, and in claim 13's lack of a detecting device. Thus, claim 13 is rejected for the same reasons as claim 5.

26. Regarding claims 6 and 14, taking claim 6 as exemplary, Seal has taught the apparatus for processing data of claim 5, wherein:

a. The outputted N-bit result from the selector and the N-bit data held in the general register bank are formed in combination as a first N-bit part and a second N-bit part of the 2N-bit addition operand (see Col.3 lines 65-67 and Col.4 lines 1-7). It has already been shown above that N-bit data is held in the general register bank, and that a selector controlled by a class signal chooses the N-bit result from one of the two register banks.

b. The accumulated result includes a third N-bit part and a fourth N-bit part (see Col.4 lines 2-4);

27. Seal has not taught that when the class signal is the second class of instruction, the detecting device compares the first N-bit part of the 2N-bit addition operand and the third N-bit part of the accumulated result to determine if the case of overflow occurs.

28. However, Morrison has taught a scaler (60 of Fig.9) which contains a comparator (see Col.9 lines 24-25). The comparator compares a portion of the expected value with the final accumulated result (see Col.9 lines 1-9) and checks for equality. It is well known in the art that here are various ways to check for overflow, such as sign checking or comparing portions of the

operands for equality or inequality, and these methods depend on the precision of the calculation being checked. Because the accumulator which holds the final result is larger than an individual operand (see Col.7 lines 61-63), one of ordinary skill in the art at the time of invention would have recognized that when checking a portion of an accumulated result for equality with the expected result, one only needs to check the most-significant bits which are larger than the operand. Also, if the expected result is also the same size as an operand, then the portion of an intermediate result, existing prior to the final addition, that is larger than an operand should remain the same through the final calculation, and thus can be compared to the final result for equality instead of calculating an expected result. Therefore, one of ordinary skill in the art would have found it obvious to compare a first portion of the accumulated result to a first portion of an intermediate result for equality when checking for overflow of an operation.

29. Claim 14 is nearly identical to claim 6, differing only in their parent claims, which are both rejected above, and in claim 14's lack of a detecting device. Thus, claim 14 is rejected for the same reasons as claim 6.

30. Regarding claim 7, Seal has taught the apparatus for processing data of claim 1, but has not taught the apparatus further comprising a detecting device, coupled to the accumulator, for receiving the 2N-bit accumulated result and for checking if a case of overflow occurs.

31. However, Morrison has taught a scalar (60 of Fig.9) connected to the accumulator (see Fig.9) that contains a comparator that determines whether the result has overflowed (see Col.9 lines 24-42). One of ordinary skill in the art would have recognized that overflow detection is desirable in order to prevent errors from propagating through a data processing system without having to recalculate operations already performed (see Col.10 lines 54-58). Therefore, one of

ordinary skill in the art at the time of invention would have found it obvious to include a comparator connected to the accumulator to detect overflow to prevent error propagation.

32. Claim 15 is nearly identical to claim 7, differing only in their parent claims, which are both rejected above, and in claim 15's lack of a detecting device. Thus, claim 15 is rejected for the same reasons as claim 7.

33. Regarding claims 8 and 16, taking claim 8 as exemplary, Seal has taught the apparatus for processing data of claim 7, wherein:

a. The outputted N-bit result from the selector and the N-bit data held in the general register bank are formed in combination as a first N-bit part and a second N-bit part of the 2N-bit addition operand (see Col.3 lines 65-67 and Col.4 lines 1-7). It has already been shown above that N-bit data is held in the general register bank, and that a selector controlled by a class signal chooses the N-bit result from one of the two register banks.

b. The accumulated result includes a third N-bit part and a fourth N-bit part (see Col.4 lines 2-4);

34. Seal has not taught that when the class signal is the second class of instruction, the detecting device compares the first N-bit part of the 2N-bit addition operand and the third N-bit part of the accumulated result to determine if the case of overflow occurs.

35. However, Morrison has taught a scaler (60 of Fig.9) which contains a comparator (see Col.9 lines 24-25). The comparator compares a portion of the expected value with the final accumulated result (see Col.9 lines 1-9) and checks for equality. It is well known in the art that here are various ways to check for overflow, such as sign checking or comparing portions of the operands for equality or inequality, and these methods depend on the precision of the calculation

being checked. Because the accumulator which holds the final result is larger than an individual operand (see Col.7 lines 61-63), one of ordinary skill in the art at the time of invention would have recognized that when checking a portion of an accumulated result for equality with the expected result, one only needs to check the most-significant bits which are larger than the operand. Also, if the expected result is also the same size as an operand, then the portion of an intermediate result, existing prior to the final addition, that is larger than an operand should remain the same through the final calculation, and thus can be compared to the final result for equality instead of calculating an expected result. Therefore, one of ordinary skill in the art would have found it obvious to compare a first portion of the accumulated result to a first portion of an intermediate result for equality when checking for overflow of an operation.

36. Claim 16 is nearly identical to claim 8, differing only in their parent claims, which are both rejected above, and in claim 16's lack of a detecting device. Thus, claim 16 is rejected for the same reasons as claim 8.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

2. Haines et al, U.S. Patent No. 5,319,588, has taught a method of detecting overflow in multiply accumulate instruction execution.

3. Dowling, U.S. Patent No. 6,370,640, has taught two register banks connected in parallel, the outputs of which are controlled by a decoder with a select signal.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
9/24/2003

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